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DESIGN AND ANALYSIS OF LOW VOLTAGE, LOW POWER FULLY RECYCLING FOLDED CASCODE AMPLIFIER

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Abstract- In this paper design of low voltage low power A fully recycling folded cascode amplifier is designed mostly all trasistors are in subthreshold region which allowes low voltage with low power dissipatioon.The proposed amplifier designed using possitive feedback technique. The proposed amplifier gives good performance over that of the conventional folded cascode (FC) amplifier. This amplifier implemented in cadence virtuoso 180nm CMOS technology and operated with a 600mV supply voltage, 900fF capacitor load. The proposed FRFC amplifier achieves 73.5dB DC gain (73.5 dB versus 55 dB) and better phase margin as 56 degrees. The amplifier consumes 7µW which make it suitable for low power bio medical applications.
Keywords- FRFC: Fully Recycling Folded Cascode, FC: Folded Cascode

1. INTRODUCTION

Operational Amplifier is an integral part of many analogue and mixed signal systems. An amplifier whose differential input voltage produces an output current. The design of amplifier continues to face challenge as the supply voltage and transistor length scale down with each newer generation of CMOS technologies. To address the issue of power efficiency, amplifier is used.

Operational amplifiers are extensively used in analog and mixed signal integrated circuits such as filters, data converters and many other applications. Among many amplifiers architectures, folded cascode amplifier is faster and give better transconductance response so it give more gain than the multi stage amplifiers. The input differential pair is the main part of operational amplifier. An amplifier means they can amplify signals in certain ratio of input to output. The ratio is commonly referred as the gain of the operational amplifier. They can be mostly used to amplify weak electrical current signals to strong electrical signals in radio, TV, and many other electrical devices..

In this paper, folded cascode amplifier with positive feedback technique is used to get good performance than the normal folded cascode amplifiers. These amplifiers are operated in ±600mv of supply voltage so transistors of amplifiers are operated mostly in subthreshold region. Subthreshold or weak inversion region means gate to source voltage is below the threshold voltage. Subthreshold region have more importance now a days because due to subthreshold the supply voltage is scaled down continuously. In sub threshold region, MOSFET has low saturation voltages to get larger output voltage swing. For this subthreshold region we get the more gain and consumes less power than the active region. This amplifier consumes <8µW of power and open loop gain = 73dB is verified by the 0.18µm CMOS technology. .

This paper organized as follows. In Section II describes folded cascode structures those are folded cascode amplifier and recycling folded cascode amplifier. Section III describes proposed amplifier i.e., fully recycling folded cascode amplifier. Section IV demonstrates simulation results and discussions. Section V shows comparative analysis with conventional ones. Finally conclusion is presented.

2. FOLDED CASCODE AMPLIFIERS

Folded cascode architecture is used for high swing and high gain with low power consumption. This op-amp uses cascodeing in the output stage. It exhibits good gain and output voltage swing, slew rate, power consumption than the two stage operational amplifier. Folded cascode amplifier has more transconductance so the dc gain is more and the common mode rejection ratio is also high, and it is easier to stabilize, since single high impedance node at output stage. Fig 1 shows schematic of folded cascode amplifier.

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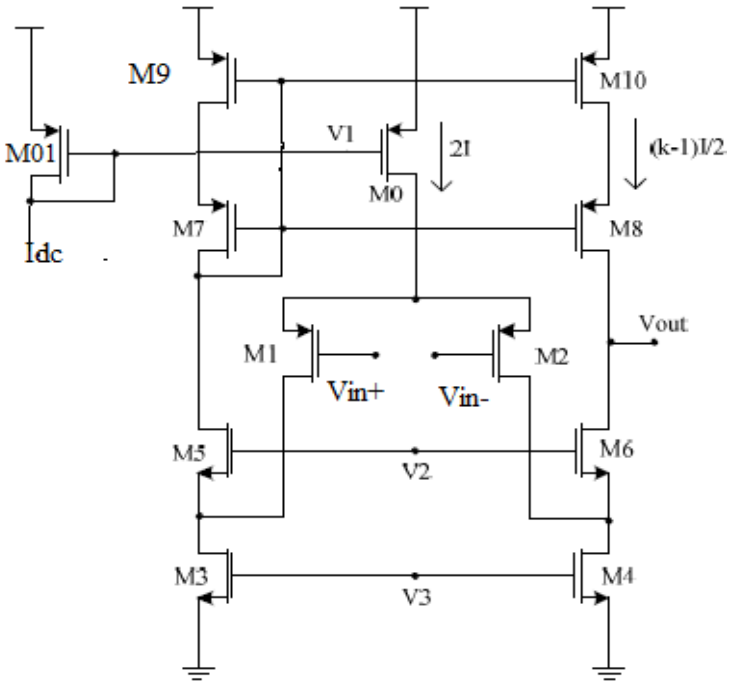

Fig 1: Folded cascode amplifier

In the above schematic the transistors M1,M2 are differential input pair. Current source is connected at M01, M0 transistors. M4, M5, M6, M7 transistors act as current mirror. Two bias voltages is given to M5, M6 and M3, M4.

Table 1: Input specifications

	Value
Vdd	0.6v
Vss	-0.6v
Unity gain frequency	>3MHz
Phase margin	55-60deg
Power consumption	<10µwatts
Slewrate	>2v/µs
CMRR	>100dB
Capacitor load	900fF

2.1 Recycling folded cascode amplifier

In order to enhance folded cascode amplifier the RFC introduced, which has advantages of higher gain and better phase margin than conventional folded cascode amplifier the work on RFC used positive feedback to enhance performance of RFC. The transconductance is increased without consuming more power. In addition with the positive feedback can be used for increasing the output impedance which leads to higher DC gain. Input transistors of folded cascode i.e. M1,M2 are split in half to produce transistors M1a,M1b,M2a,M2b this will conducts fixed and equal currents. M3 and M4 are split to form current mirror M3a,M3b,M4a,M4b. The cross over connections of these current mirrors insures small signal currents added to source of M5 and M6 which are in phase. M11 and M12 are sized similar to M5 and M6 and the addition of it helps to maintain drain potentials of M3a and M3b & M4a and M4b. The following schematic shows the recycling folder cascode amplifier.

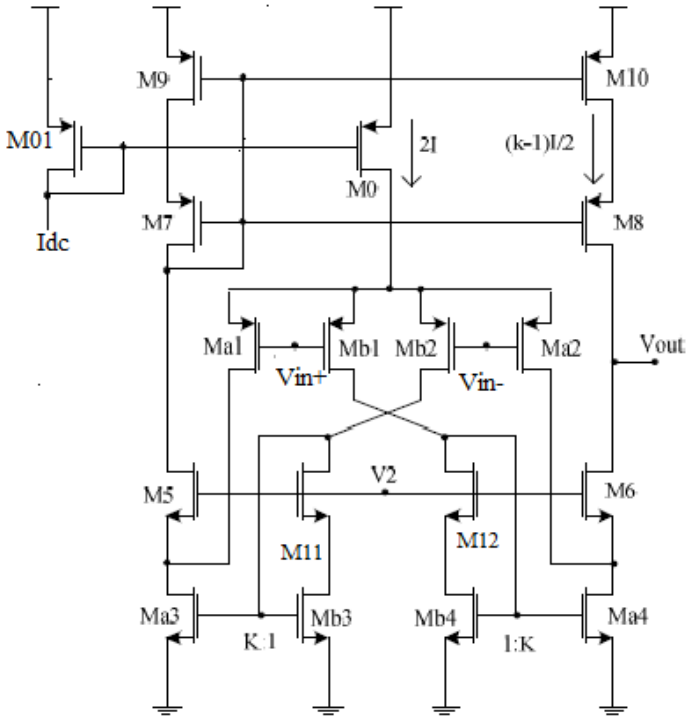

Figure2: Recycling Folded Cascode amplifier

3. FULLY RECYCLING FOLDED CASCODE AMPLIFIER

In FERFC M9&M10 as driving transistors, a cross over connection between Mb3& Mb4 with M9 and M10 established. To maintain amplifier as single ended architecture M11 and M12 are added. Ma3, Mc1, Mb3 act as high speed current mirrors in this a compensation resistor is used to maintain amplifier as more stable. The following schematic shows the fully recycling folded cascode amplifier. The amplifier's transconductance (Gm) is found by calculating short-circuit current at the output with regards to the input. As mentioned previously, the M1 is the twice the size of Ma1 and conducts twice the amount of current ($gm_1=2gm_{a1}$).

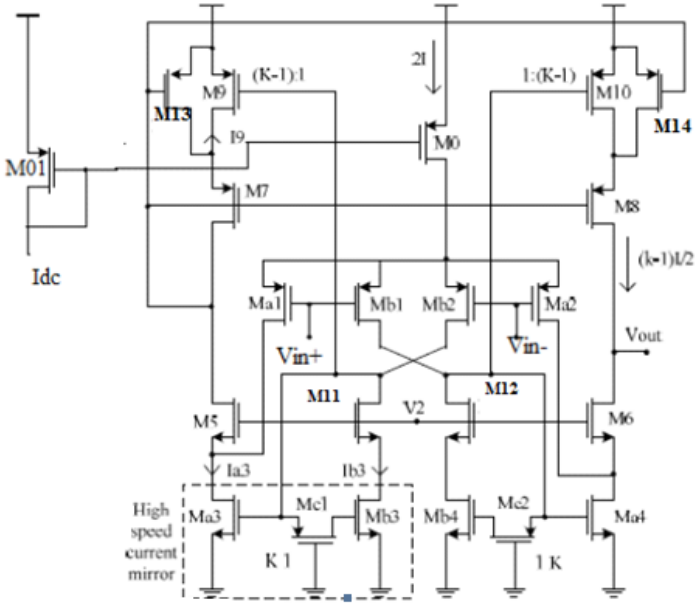

Figure3: Fully Recycling Folded Cascode Amplifier.

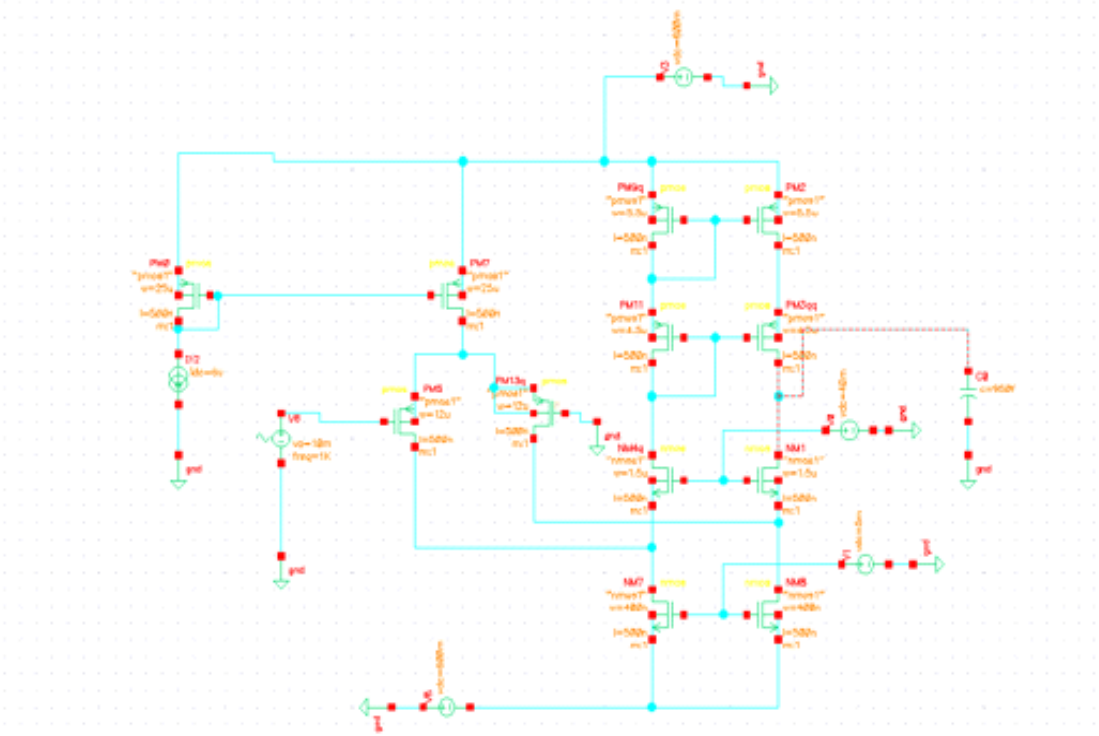

Figure4: Schematic of Folded Cascode Amplifier.

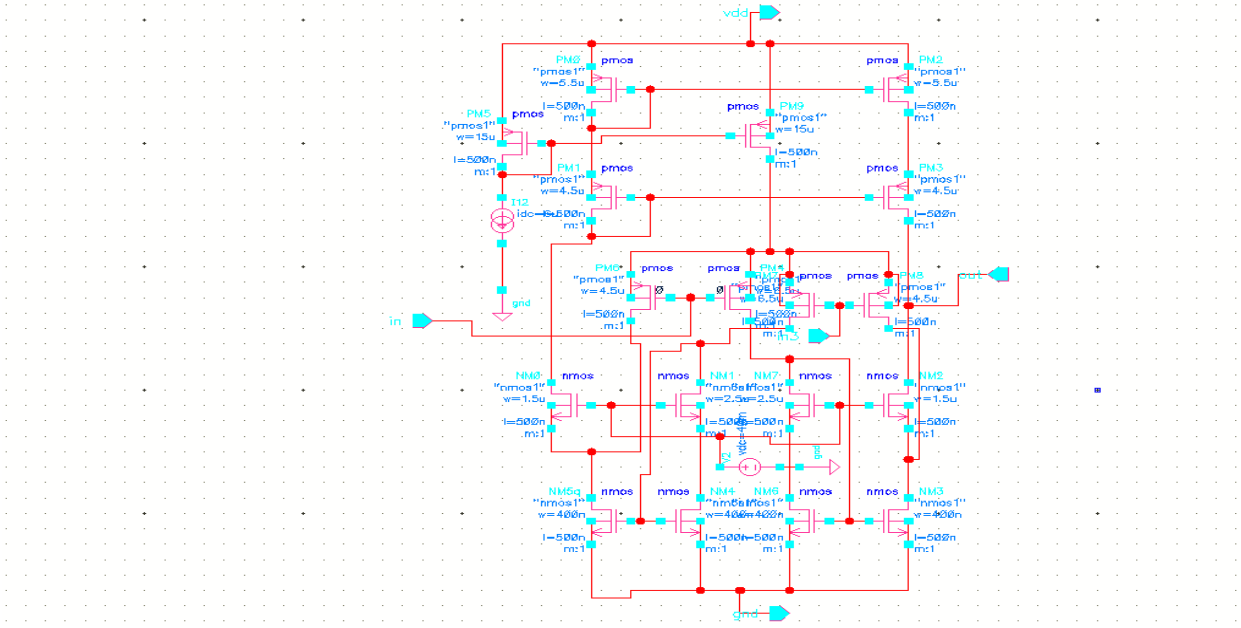

Figure5: Schematic of Folded Cascode Amplifier.

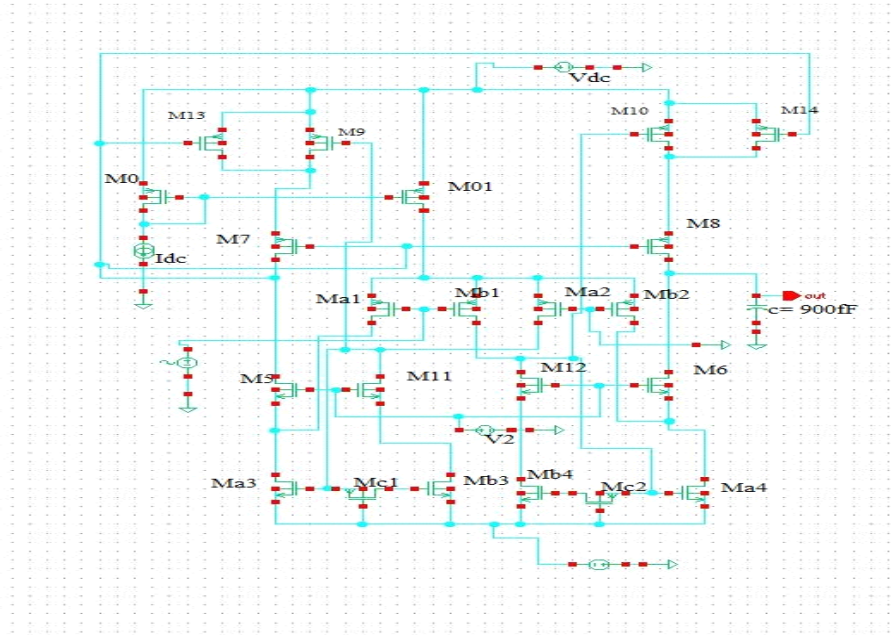

Figure 6: Schematic of Fully Recycling Folded cascode amplifier

In the above schematic sinusoidal signal applied as input signal to differential input pair. Current source is given as 6µA. Transistors M1a, M1b, M2a, M2b introduce positive feedback and increase effective transconductance.

4. RESULTS AND DISCUSION OF FULLY RECYCLING FOLDED CASCODE AMPLIFIER

Simulation Results of the above circuits using Cadence Virtuoso simulator are

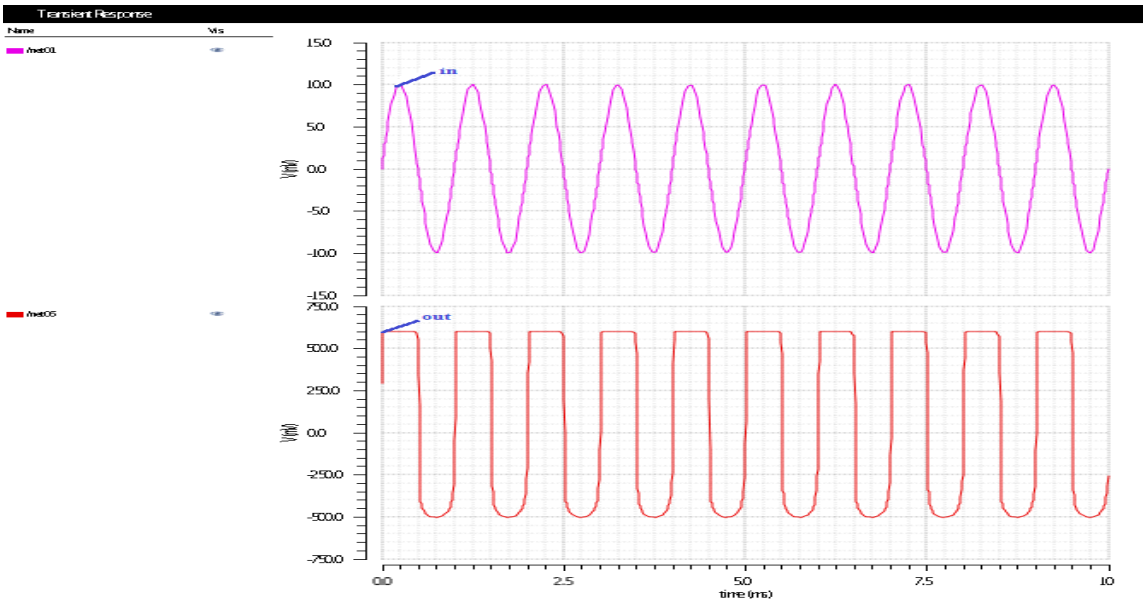

Figure 7:Transient response

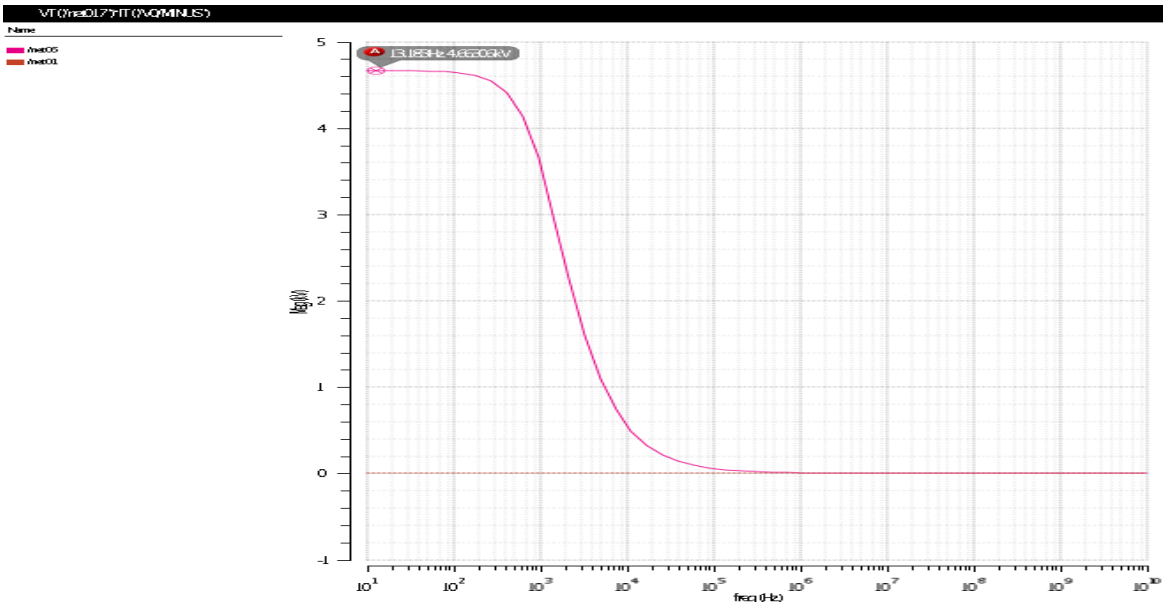

Figure 8:ACresponse

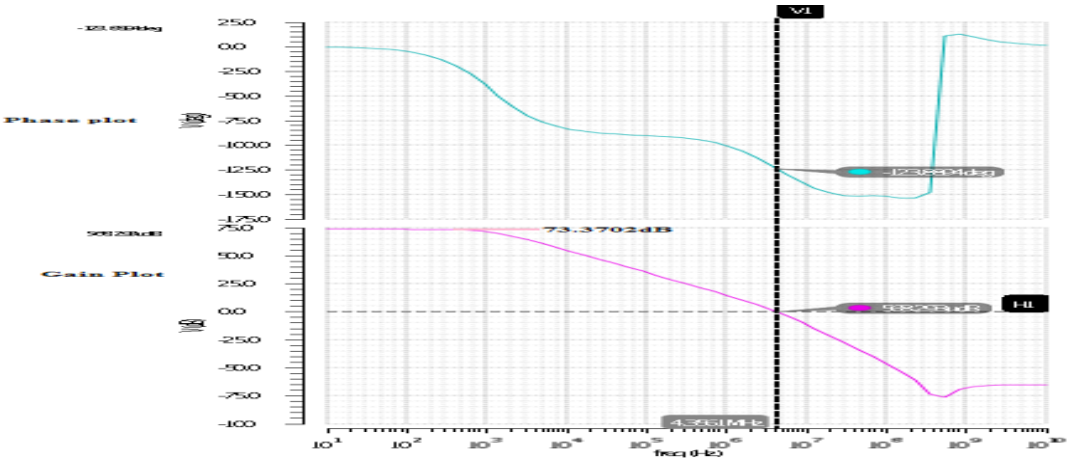

Figure 9: Gain And Phase response

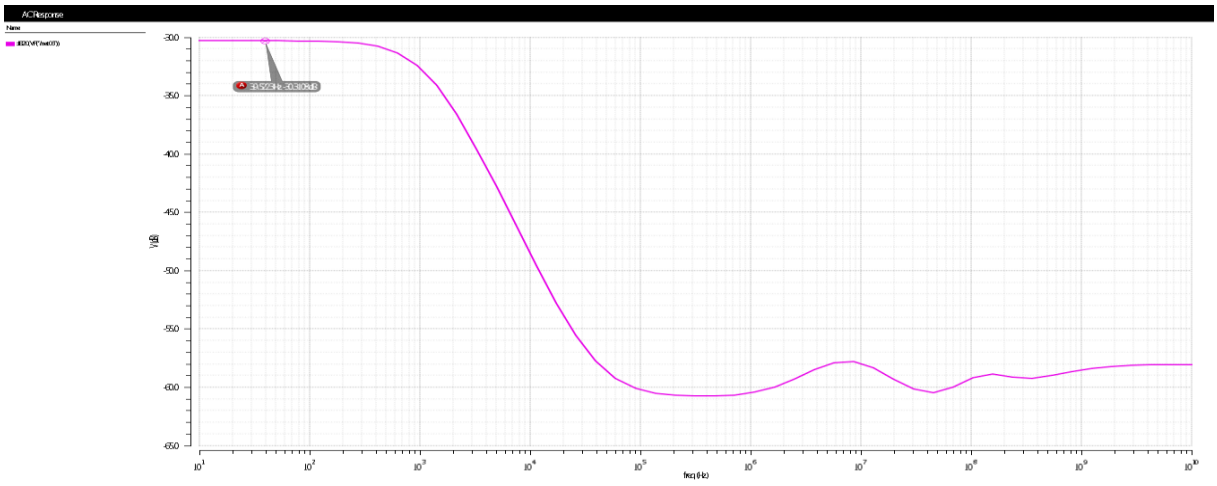

Figure 10: Common mode Gain

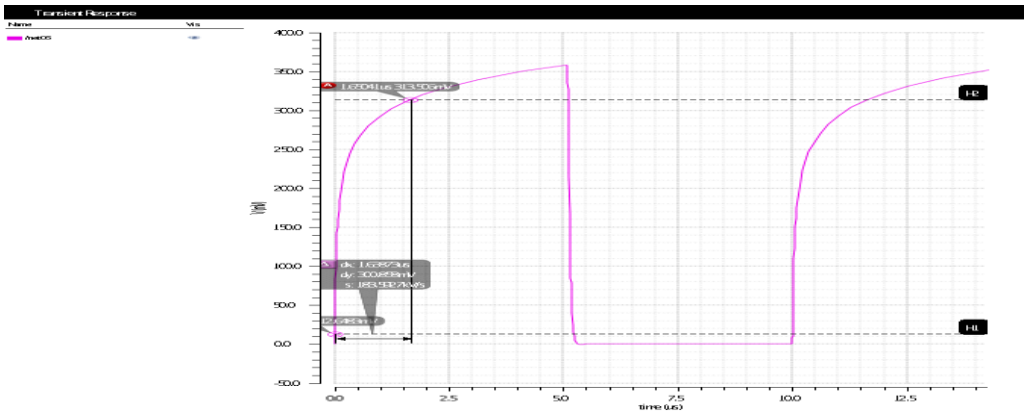

Figure 11: Positive Slew rate response

SR+ =183.68V/ms
=0.183v/µs

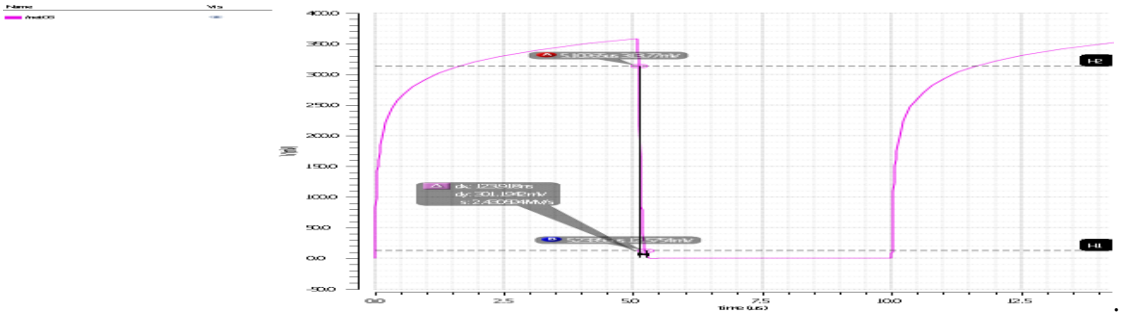

Figure 12: Negative Slew rate response .

SR- =2.4309V /us
total slew rate= SR+ +SR-
=0.183v/µs+2.4309V/µs=2.6139V/µs.

The below table shows the comparison of each parameter of proposed amplifier with the conventional amplifiers. Itshowsthat proposed amplifier gives Gain of 73dB withhigh CMRR and better slew rate compared to the conventional Folded cascode amplifier. The proposed amplifier consumes less power compared with conventional amplifier
The creation of mask layout is one of the important steps in the full custom design flow, where the designer describes the detailed geometry and the relative positioning of each mask layer to be used in actual fabrication, using a layout editor.

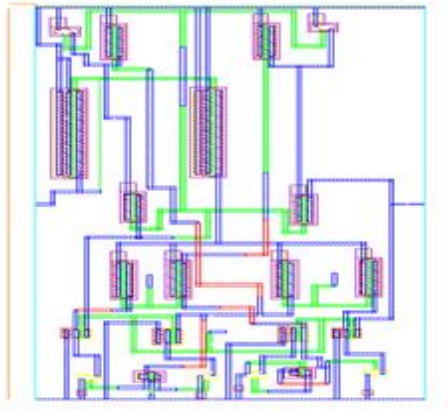

Figure13: Layout of Proposed Amplifier.

Layout must be drawn according to strict design rules. After you have finished our layout, an automatic program will check each and every polygon in the design against these design rules and report violations. This process is called Design Rule Checking and must be done for every layout to ensure that it will function properly when fabricated. The next step is to

compare the net list extracted from the layout with the schematic to ensure that layout drawn is an identical match to the cell schematic.

5. COMPARATIVE ANALYSIS AND CONCLUSION

Table2: Comparative analysis of simulation results of folded cascode amplifiers

Performances	Folded Cascode Amplifier	RFC Amplifier	Proposed Amplifier
Technology(nm)	180	180	180
Power supply(mV)	600	600	600
Open loop gain (dB)	55	68.52	73.26
Phase Margin (degrees)	81.6	80	57
Unity gain bandwidth (MHz)	7.103	8.301	4.3227
CMRR (dB)	67.96	90.52	103.52
SR (v/µs)	3.103	3.122	2.6139
PSRR+ (dB)	84.27	99.89	103.12
PSRR- (dB)	150.9	100.15	79.337
Power (µW)	7.443	7.443	6.99

In this paper, The design of a low power and high gain CMOS Folded cascode amplifier is proposed, which can be used for bio-medical and low power applications. This design is carried out in CMOS 180nm technology, with the supply voltage of 600mv. The circuit is operated in sub threshold region. The standard current mirror circuit is connected to make the current constant irrespective of the output load. This amplifier gives gain of about 73dB with the effective CMRR of 103dB and phase margin 56deg with low power consumption of 7µwatts.

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